Low-Power Fully Differential Ultra-Wide Band CMOS Multiplier for FM-UWB and IR-UWB Systems

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Abstract

A CMOS low-power four-quadrant multiplier for Ultra-Wide Band (UWB) systems using FM-UWB and Impulse Radio (IR) is presented. A set of transconductors, rather than the traditional Gilbert cell, is employed. The configuration is simple and area saving. The simulated result shows: An average gain of 22.5 dBV^{-1} *and* 20.8 dBV^{-1} *in the bandwidth of* 700 *MHz at* 1.2 *GHz and* 4 *GHz center frequencies, respectively,* 1.8 *mA total current with* 2.5 *V power supply, and a linear range of* $\pm$900 *mV. The layout area of the proposed multiplier*[1] *is approximately* 200 $\mu m \times$ 300 μm. *The process is the UMC* 0.25 μm *standard CMOS process.*

Keywords: UWB, FM-UWB, IR-UWB, short-range personal communication, CMOS four-quadrant multiplier.

1 INTRODUCTION

Short-range communication is likely to be a main stream field of research in the next couple of decades [1]. Being the basic physical support of short-range personal communication, UWB RF front-end circuit technology will also be a central point in the circuit design area. So far the UWB RF front-end configuration adopts two concepts: FM-UWB and IR-UWB. In both configurations, the multiplier plays an important role in demodulation and signal detection.

Bandwidth, gain and linearity are the basic requirements for UWB multipliers from a system point of view. Considering that in most cases, the personal short-range electronics devices are portable and battery powered, the power consumption and cost are crucial factors in block design.

The well-known Gilbert cell is a popular multiplier topology being implemented in bipolar IC technology giving wide dynamic and frequency range [2, 3]. The Gilbert cell implemented in CMOS technology has also been published, e.g. [4, 5]. However, due to the differences between bipolar and MOS devices while considering cost, circuit complexity and integration with digital blocks, the CMOS multiplier seems to be an attractive technology for UWB-devices. Because of limitations of CMOS devices with regards to noise and linearity performance, CMOS UWB multiplier design is still a challenging task for low cost, low-power applications.

In this paper, Section 2 discuss the circuit description and theory of the proposed multiplier as well as the parameter definition for the simulated results, which are presented in Section 3. Finally, a conclusion is drawn in Section 4.

2 CIRCUIT DESCRIPTION AND THEORY

As illustrated in Fig. 1, the multiplier consists of two pairs of transconductors [6]. A buffer is also employed for impedance isolation and matching. The bias system is not shown. x and y are differential input signals. The differential structure ideally removes common-mode (CM) signals and mitigates the effect of even-order non-linear terms.

While all transistors are properly biased by voltages X and Y, the bottom transistors (M1 – M4) and the upper transistors (M5 – M8) operate in the linear and saturation regions, respectively. Each of them has the same aspect ratio. M9 and M10 are buffer PMOS transistors operating in the saturation region.

Recall the I-V characteristic of a NMOS in the linear region:

$$I_{ds} = \beta[(V_{gs} - V_{tn})V_{ds} - \frac{V_{ds}^2}{2}] \quad (1)$$

and in the saturation region:

$$I_{ds} = \beta(V_{gs} - V_{tn})^2 \quad (2)$$

[1]The design has been sent for tapeout and the test result will be presented at the conference.

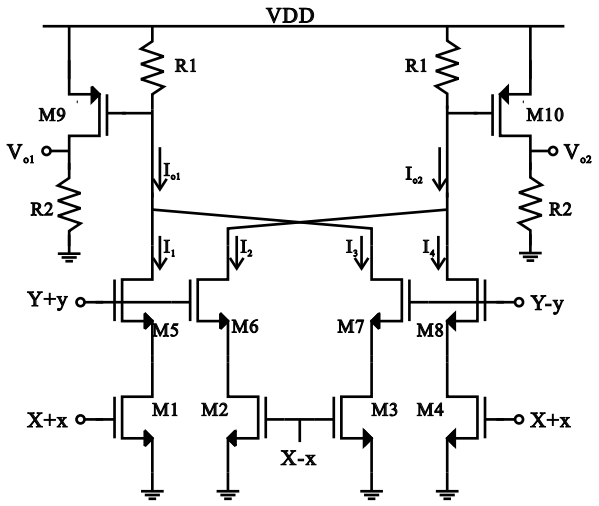

Figure 1: Proposed low-power CMOS four-quadrant multiplier core with buffers.

where $\beta = \mu_n C_{ox}\left(\frac{W}{L}\right)$ and V_{tn} is the transconductance and the threshold voltage of the MOS transistor, respectively.

The upper transistors in Fig. 1 are all assumed to be source followers. While having all transistor sizes equal and making the above assumption true, it is important that all transistors operate at a low current. Thus, V_{ds} of the transistors in the linear region is a function of y through the upper transistors. They can be expressed as:

$$V_{ds1} = V_{ds2} = Y' + y \quad (3)$$
$$V_{ds3} = V_{ds4} = Y' - y \quad (4)$$

where $Y' = Y - V_{gs_{upper}}$ and $V_{gs_{upper}}$ is the gate-source voltage of the upper transistors.

When the bottom transistors operate in the linear region, from Eq. (1) the channel currents can be written as:

$$I_1 = \beta[(X + x - V_{tn})(Y' + y) - \frac{(Y' + y)^2}{2}] \quad (5)$$
$$I_2 = \beta[(X - x - V_{tn})(Y' + y) - \frac{(Y' + y)^2}{2}] \quad (6)$$
$$I_3 = \beta[(X - x - V_{tn})(Y' - y) - \frac{(Y' - y)^2}{2}] \quad (7)$$
$$I_4 = \beta[(X + x - V_{tn})(Y' - y) - \frac{(Y' - y)^2}{2}] \quad (8)$$

From the above equations, the total output current yields:

$$\begin{aligned} I_{out} &= I_{01} - I_{02} \\ &= (I_1 + I_3) - (I_2 + I_4) \\ &= \beta[2XY' + 2xy - 2V_{tn}Y' - (Y')^2 - y^2] - \\ &\quad \beta[2XY' - 2xy - 2V_{tn}Y' - (Y')^2 - y^2] \\ &= 4\beta xy \end{aligned} \quad (9)$$

If the output current flows through an output stage with a total impedance, Z_{out}, then the output voltage will result in

$$V_{out} = -I_{out}Z_{out} = -4xy\beta Z_{out} \quad (10)$$

So,

$$V_{out} = K \cdot xy \quad (11)$$

where

$$K = -4\beta Z_{out} \quad (12)$$

Therefore, the multiplication function can be obtained.

The following section defines the gain and the linearity of the multiplier used in the simulations.

Consider two input voltage signals:

$$x(t) = A_x \cos(2\pi f_x t) \quad (13)$$
$$y(t) = A_y \cos(2\pi f_y t) \quad (14)$$

where A_x and A_y are the amplitude of $x(t)$ and $y(t)$, respectively. Applying the above signals to the multiplier yields:

$$\begin{aligned} v_{out}(t) &= K \cdot A_x \cdot A_y \Big(\frac{1}{2} \cos\big(2\pi(f_x - f_y)t\big) \\ &\quad + \frac{1}{2} \cos\big(2\pi(f_x + f_y)t\big) \Big) \end{aligned} \quad (15)$$

Since the multiplier is used in the receiver, the only concern from the above condition is the lower frequency part ($f = f_x - f_y$) of $v_{out}(t)$, $v_{out_{LF}}(t)$.

$$v_{out_{LF}}(t) = A_{out_{LF}} \cos\big(2\pi(f_x - f_y)t\big) \quad (16)$$

where

$$A_{out_{LF}} = \frac{KA_xA_y}{2} \quad (17)$$

Thus, the gain of the multiplier is defined as:

$$\text{GAIN} = 20\log\left(\frac{A_{out_{LF}}}{A_x \cdot A_y}\right) \quad (18)$$
$$= 20\log(\frac{K}{2}) \quad [dBV^{-1}] \quad (19)$$

From Eq. (12), the gain of the multiplier is related to β as well as Z_{out}. Assuming that Z_{out} and the gate bias voltages are held constant, then a larger the transistor size gives a higher gain, and the more total

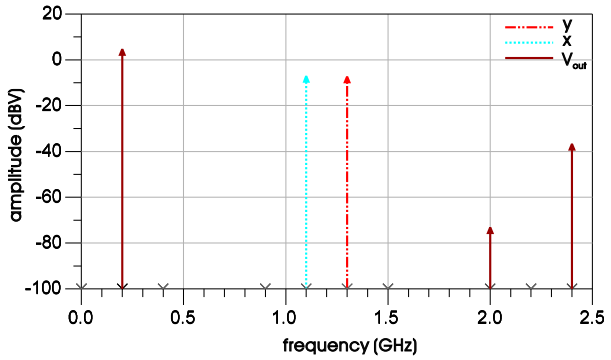

Figure 2: Simulated output spectrum when two sine wave signals are applied to the proposed multiplier (Fig. 1) at 1.1 and 1.3 GHz, respectively.

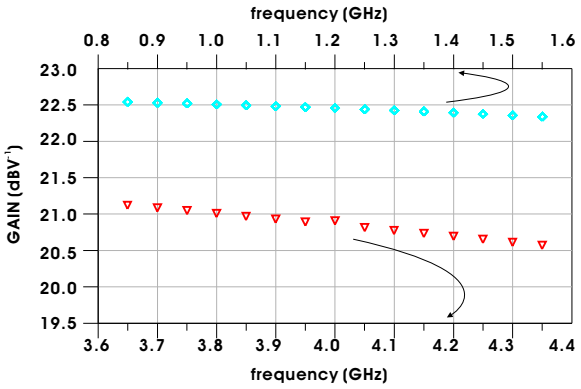

Figure 3: Simulated gain of the multiplier centered at 1.2 GHz and 4 GHz.

current is consumed. This is a major tradeoff between the gain and the current. In addition, the bandwidth of the multiplier is subject to the characteristic of the MOS parameters; in particular, the gate-to-source capacitor (C_{gs}).

To define the linearity of the multiplier, a two-tone signal, Eqs. (13) and (14), are applied to the multiplier. A sweep of A_x from -0.3 V to 0.3 V at $A_y = -300$ mV is carried out at a fixed biasing condition. An extrapolation using the slope of the linear part of the curve is performed. These two curves are then calculated for a deviation in percentage using:

$$\text{deviation} = \left(\frac{|\text{ND} - \text{ELD}|}{\text{ELD}}\right) \times 100 \quad [\%] \quad (20)$$

where ND and ELD is the actual data from the sweep and the extrapolated linear data of ND, respectively.

The linearity of the multiplier is defined by the range of the DC output voltage at 10% deviation from the extrapolated linear data. The simulation results shown are obtained using ideal voltage sources for the x- and y-inputs. Using other source impedances may influence the results.

3 SIMULATION RESULTS

The proposed multiplier circuit in Fig. 1 was simulated using ADS (Advanced Design System) with UMC 0.25 μm CMOS technology. The transistors (M1−−M8) are biased using a CMOS current mirror. The output stage uses two N+ polysilicon resistors with a PMOS transistor. All models for NMOS and PMOS used in the simulation are from the UMC design kit. The power supply is 2.5 V, and the total current to the circuit is approximately 1.85 mA. The layout is shown in Fig. 5.

Fig. 2 shows the spectrum of the multiplier in the frequency domain, where x and y are sine waves at 1.1 GHz and 1.3 GHz, respectively. The corresponding output of the multiplier has two signal components plus higher order products. Both 1.1 and 1.3 GHz input signals have the amplitude of -3.78 dBV, whereas the amplitude of the output signal at 200 MHz has 2.1 dBV. Adding capacitors at the outputs of the multiplier can filter out unwanted signals.

Fig. 3 shows the simulated gain performance of the multiplier at two different center frequencies, 1.2 GHz and 4 GHz, and the corresponding gains are at an average of 22.5 dBV^{-1} and 20.8 dBV^{-1}. A_x and A_y are fixed to 200 mV, which is within the linear range of the multiplier. The gain depends on β and Z_{out}. In the bandwidth of approximately 700 MHz, their gain deviations are $\pm$0.3 dB and $\pm$0.6 dB, respectively. The testing condition utilizes two identical sine waves with the same frequency and phase.

Fig. 4a shows the simulated linearity of the multiplier, where the deviation plot of the first four DC curves is shown in Fig. 4b. Both inputs (x and y) are two identical sine waves with frequency 1.25 GHz and their amplitudes are swept from -300 mV $\sim$ 300 mV. From curve #1 in Fig. 4b, when A_x is swept from -300 mV to 300 mV at A_y equal to $\pm$300 mV, the corresponding output DC voltage has the linear range from -900 mV to 900 mV.

From the simulation results, the proposed multiplier has demonstrated a low-power high-gain performance for UWB applications. CMOS four-quadrant analog multipliers for either a wide bandwidth ($<$ 103 MHz) at a centre frequency close to 1 GHz or low-power (0.6 $\sim$ 2.8 mW) application using 0.8 μm and 1.2 μm process have been reported in [2], [3]. Using the same configuration for both wide bandwidth and low power application at the UWB operational band has not been reported in the research field.

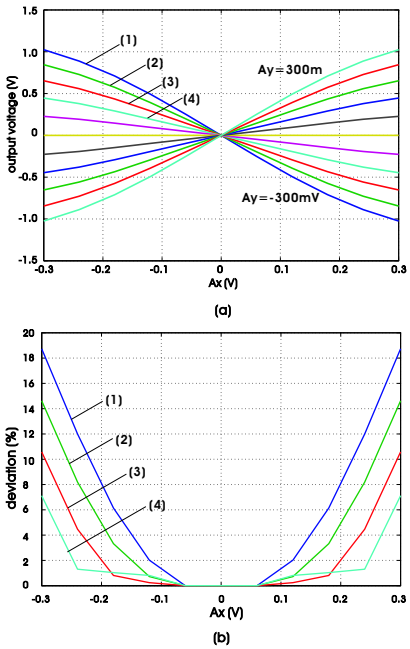

Figure 4: (a) DC characteristics of the multiplier. (b) Deviation plots of the first four DC curves. From curve #1, when A_x is swept from -300 mV to 300 mV at A_y equal to ±300 mV, the corresponding output DC voltage has the linear range within 10 % deviation from -900 mV to 900 mV.

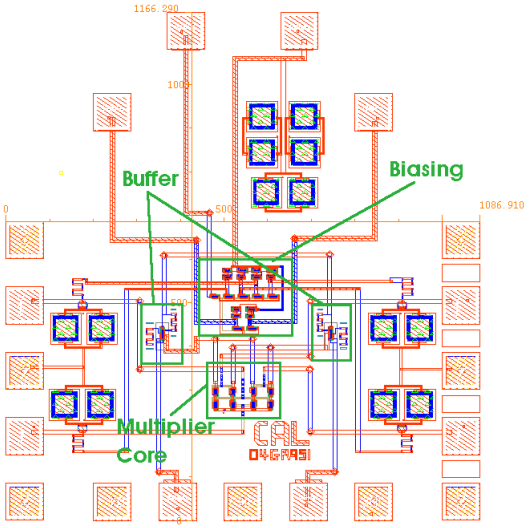

Figure 5: Layout of the whole multiplier design which includes the pads, decoupling capacitors, matching components, biasing circuit, buffer, and multiplier core. The total area is 1167 μm × 1087 μm. The area of the multiplier core is approximately 200 μm × 300 μm.

4 CONCLUSION

UWB RF front-end configuration compatible to FM-UWB and IR-UWB for short-range communication is playing an increasingly important role in circuit design area. In particular, multiplier is an essential block in demodulation and signal detection. This paper presents the first emerging CMOS low-power four-quadrant multiplier for FM-UWB or IR-UWB using UMC 0.25 μm standard process. The simulations shows a high average gain of 22.5 dBV^{-1} and 20.8 dBV^{-1} in the bandwidth of 700 MHz at the center frequency 1.2 GHz and 4 GHz, respectively. The total current consumption is 1.8 mA with 2.5 V power supply. The linear range within 10 % deviation is ± 900mV. The layout area of the multiplier cell is 200 μm × 300 μm.

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